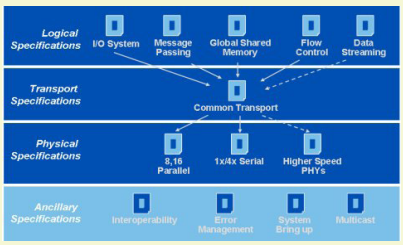
RapidIO®

The Embedded Fabric Choice

RapidIO Interconnect Benefits

- Embedded interconnect optimized by the embedded community for the embedded community
- Ideal for true networking peer-to-peer clusters of embedded processors
- Every endpoint manages its own memory system
- Wide ecosystem of microprocessors, FPGAs, DSPs, switches , OEM ASICs, boards and software support
- Lowest latency switches in industry
- Ideal for distributed computing systems with backplane oriented architectures
- 3-layer protocol terminated in hardware, freeing up processor cycles for implementing applications
- Support reliable transmission
- RapidIO Specified in PICMG 3.5 for ATCA/MicroTCA
- RapidIO Specified in VITA/VXS/Open VPX

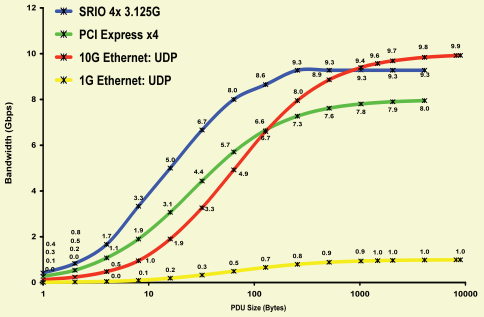


Typical Applications

- Wireless: Baseband cards and backplanes in LTE/WiMAX/WCDMA/TD-SCDMA
- Defense & Aerospace: radar, sonar nav systems
- Video and imaging
- Industrial control systems
- Storage

Comparison with Other Interconnect Protocols

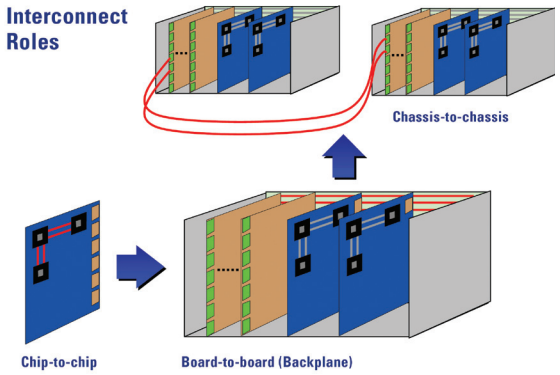
- Highest performance serial interconnect with up to 6.25 Gbaud per link
- Highest protocol efficiency in embedded systems with 94% payload vs header efficiency
- Serial RapidIO standard supports arbitrary system topology with true peer-to-peer networking
- Twice the performance per link compared to 10 Gb Ethernet
- RapidIO messaging support for transfers of large blocks of data, superior to PCIe and 10 GbE in target applications



RapidIO® Overview

The RapidIO Interconnect Architecture, designed to be compatible with the most popular integrated communications processors, host processors, and networking digital signal processors, is a high-performance, packet-switched, interconnect technology. It addresses the high-performance embedded industry's need for reliability, increased bandwidth, and faster bus speeds in an intra-system interconnect.

The RapidIO interconnect allows chip-to-chip and board-to-board communications at performance levels scaling from 1 Gigabit per second per link to as much as 80 Gbps. RapidIO is now over 10 years old and is supported by the leading semiconductor companies worldwide and has a wide, installed base of production systems in a variety of applications.



RapidIO® Technology Roadmap

The RapidIO Trade Association has a technology roadmap that provides details about RapidIO Specification Gen 2, and previews the development of Specification Gen 3, which will continue to be defined collaboratively. While the current standard (Specification Rev. 1.3) will continue to dominate embedded applications, silicon using the latest revision will debut in 2010. The embedded systems market has a stable and longer lifecycle than PC and Consumer markets, the needs of this market are reflected in the collaborative efforts of the association's members to develop the appropriate technology, cost, and performance in a timeframe suitable for the needs of its members. Details can be found at http://www.rapidio.org/education/Roadmap.

RapidIO Specification 1.3 Feature Overview

- 1.25, 2.5, 3.125 Gaud speeds
- Links of x1 and x4 configuration
- 8b/10b encoding
- Up to 10 Gbps per link
- Supports all topologies including star, dual star and mesh
- Multicast support
- Messaging support
- Reliable transmission
- Error management support
- Flow Control Extensions
- Transparent to existing software
- Flexible method for memory mapping systems
- Four priorities for improved QoS and traffic management

RapidIO Gen 2 Feature additions

- New higher performance physical layer
- 5.0 and 6.25Gbaud rates added with DFE
- Mode to facilitate short 5Gbaud links without DFE and with the IDLE1 control symbol
- Increased robustness of the IDLE2 operation
- 2x, 8x, and 16x link width options added
- Data scrambling and new control symbol functionality added
- Significant data plane enhancements
- Virtual Channels (VCs) added to Serial Physical Layer
- Virtual Output Queue (VoQ) specification
- Data Streaming Packet Format (Type 9 packet)
- New end-point flow control arbitration and traffic management

Membership Benefits

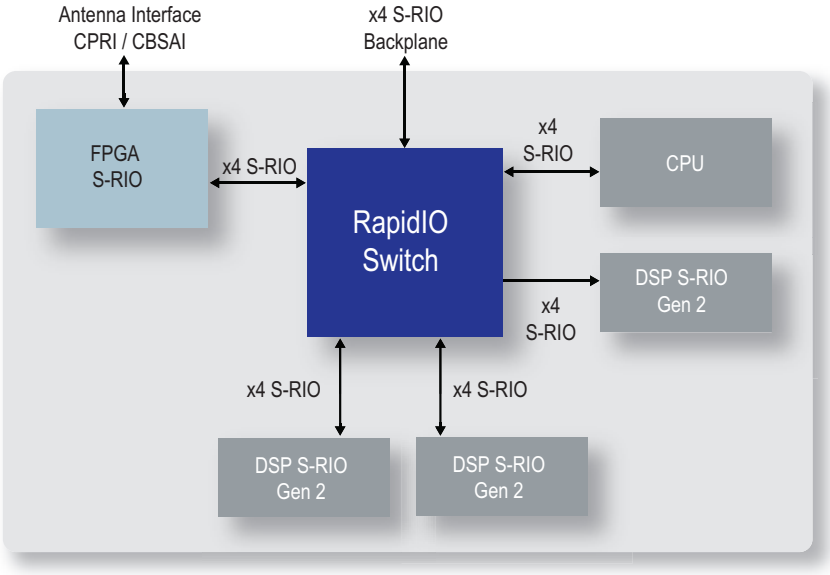
- Early access to specifications in development
- Drive new technology for your application
- Participate at RapidIO Trade Association market and customer events
- Voting privileges
- Device Vendor ID for hardware
- Access to RapidIO Bus Functional Model
- Chair working groups
- Understand where industry and peer companies are going with respect to future interconnect and application needs
- Inclusion in RapidIO Trade Association collateral

For more information, visit us at www.rapidio.org

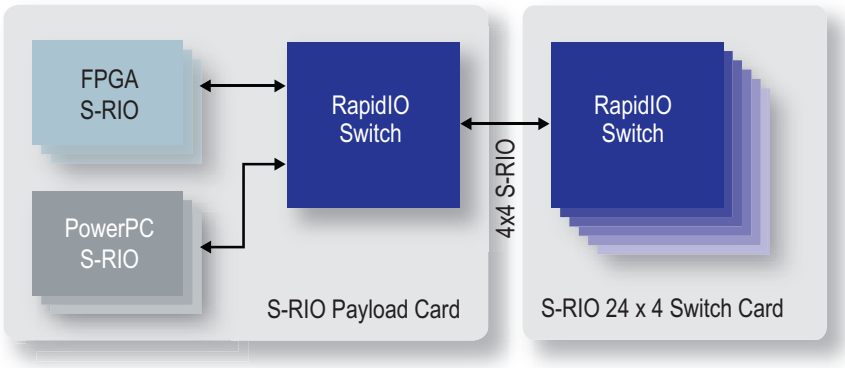
Application Views with RapidIO

RapidIO is ideal for any embedded system where the application is partitioned over multiple processing nodes. The more processors in the system, the better the performance of a RapidIO Network. Typical system architectures in Wireless and Military are shown below.

Wireless Application



Military Open VPX System



About the RapidIO Trade Association

The RapidIO Trade Association, a non-profit corporation controlled by its members, directs the development and drives the adoption of the RapidIO architecture. The trade association brings together the right ecosystem to help developers build embedded systems using the RapidIO architecture. Developers will find that the RapidIO ecosystem offers a critical mass of products on the market today – including a wide assortment of end-points – which can minimize the amount of bridging required in a design. The RapidIO membership represents a 'who's who' of leading embedded companies. Companies interested in being part of this best-in-class team are invited to join the RapidIO Trade Association. Members of the association have access to the RapidIO architecture specifications, are able to participate in specification development, and can attend all member meetings.